



CS5212 Datasheet

DisplayPort to VGA Convertor

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Contents

1	Introduction.....	5
2	Features.....	6
3	Pin Definition.....	7
3.1	Pin Assignments.....	7
3.2	Pin Description.....	8
4	Interfaces and Capability.....	9
4.1	DisplayPort Input.....	9
4.2	Analog VGA output.....	9
5	Electrical Specifications.....	11
5.1	Absolute Maximum Conditions.....	11
5.2	Operating Conditions.....	11
5.3	Electrical Specification.....	11
5.4	CS5212 Power Consumption.....	13
6	Package Specification.....	14
7	Ordering Information.....	15
8	Revision History.....	16

List of Figures

Figure 1-1 CS5212 Block Diagram.....	5
Figure 3-1 CS5212 Pin Layout	7
Figure 6-1 CS5212 Package Outline (QFN32 Leads 4x4mm ²)	14

List of Tables

Table 3-1 CS5212 Pin Definitions.....	8
Table 4-1 Supported Popular Timing/ Resolution	10
Table 5-1 Absolute Maximum Conditions	11
Table 5-2 Normal Operating Conditions.....	11
Table 5-3 DC Electrical Specification	11
Table 5-4 AC Electrical Specification.....	12
Table 5-5 CS5212 Typical Power Consumption	13
Table 6-1 Package Dimension.....	14
Table 7-1 CS5212 Ordering Information.....	15
Table 8-1 Document Revision History	16

1 Introduction

The CS5212 DisplayPort to VGA converter combines a DisplayPort input interface and an analog RGB DAC output. The embedded MCU is based on an industrial standard 8051 core.

The CS5212 is suitable for multiple market segments and display applications, such as laptop, motherboard, desktop, dongle, and docking system.

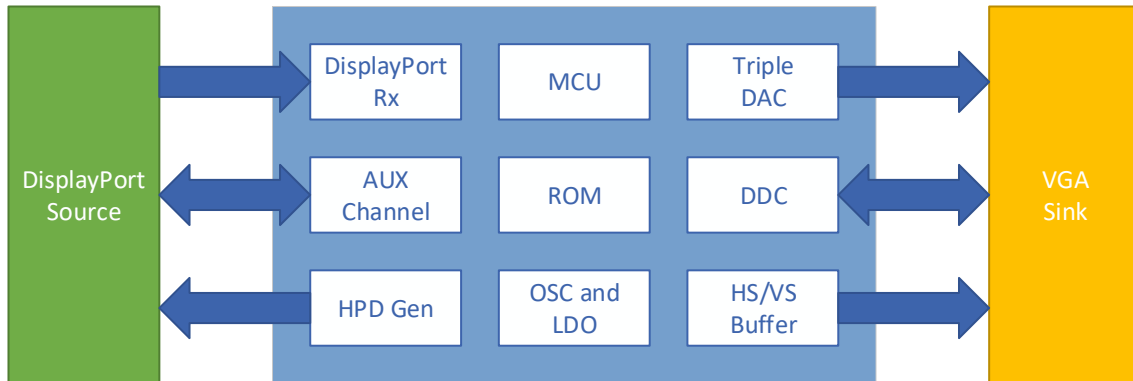


Figure 1-1 CS5212 Block Diagram

2 Features

General

- 2-lane VESA DisplayPort v1.1 compliant receiver
- VGA output interface, DAC speed up to 210-MHz, 8-bit
- Max. resolution up to 1920x1200x60 (RB, reduced blanking) with 24-bit color depth, 1920x1440x60 (RB, reduced blanking) with 18-bit color depth, or 2048x1152x60 (RB, reduced blanking) with 24-bit color depth, or 2048x1536x60 (RB, reduced blanking) with 18-bit color depth.
- Embedded oscillator and there's no need for the external crystal
- Embedded linear dropout regulator (LDO)
- Embedded MCU
- Embedded EDID (CS5212 will response EDID if terminal device doesn't have it)
- Embedded V-sync/H-sync 5V buffer
- Support EEPROM Free mode by using the internal pre-blew ROM
- Internal power-on-reset (POR)
- QFN32 4x4 package
-

DisplayPort Digital Input

- Support 2-lane digital input, speed up to RBR(1.62-Gbps) / HBR (2.7-Gbps)
- VESA DisplayPort v1.1 compliant
- Built-in high-performance adaptive equalizer
- Support 1-MHz AUX channel
- Support HPD
-

VGA Output Interface

- Triple 8-bit DAC (Digital-to-Analog Converter) with clock up to 210-MHz
- Support up to 1920x1200x60, 1920x1440x60 (reduced blanking), 2048x1152x60 (reduced blanking), and 2048x1536x60 (reduced blanking)
- Embedded V-sync/ H-sync 5V buffer
- HBM 4-KV for VGA connector pins
- VESA VSIS v1r2 compliant

Embedded MCU

- Industrial standard 8051 core
- Support I2C Master and Slave up to 400-KHz.

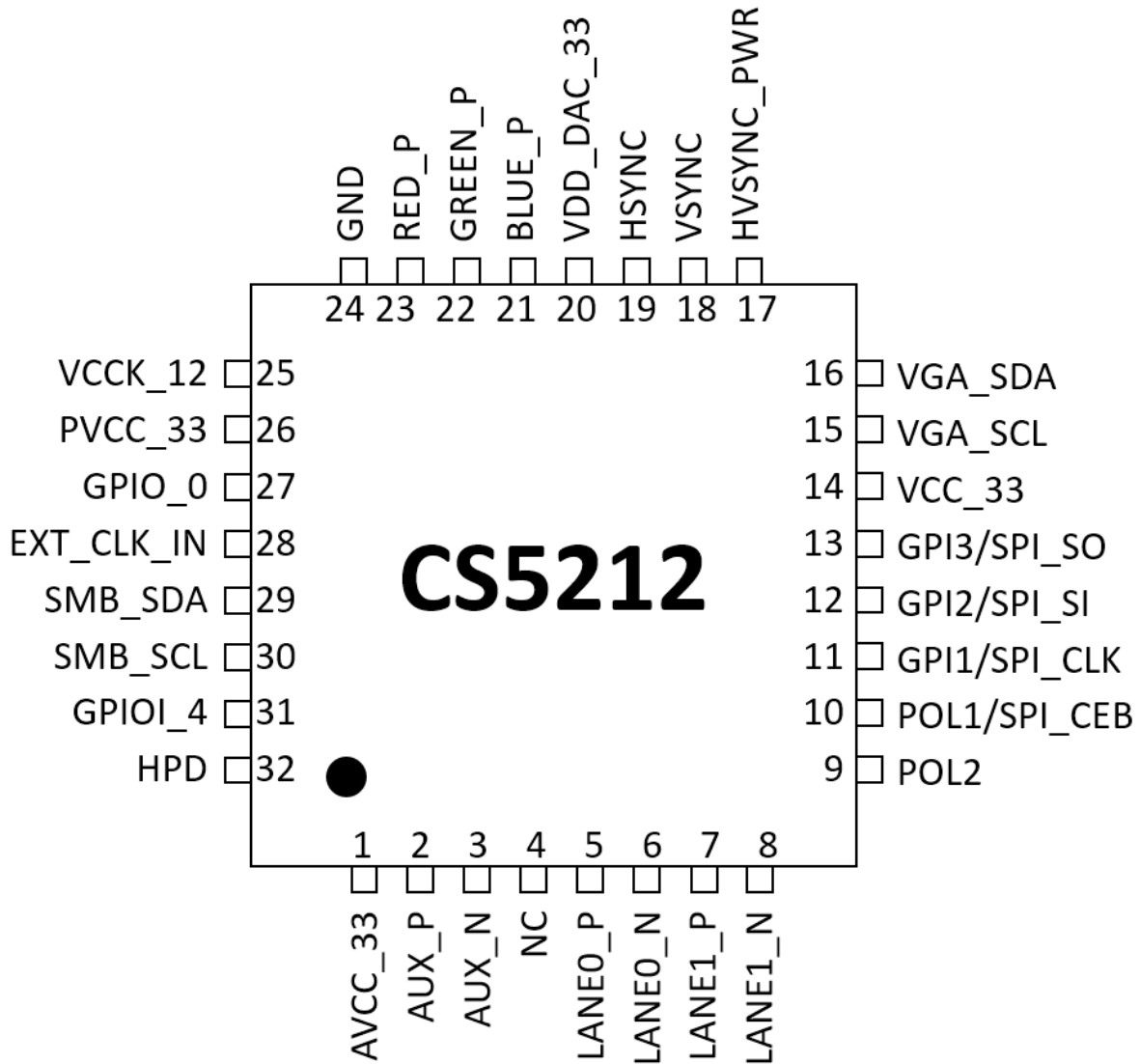
Power & Technology

- Single 3.3V power supply
- 5V Option for V-sync/ H-sync 5V buffer
- Ultralow standby power < 100uW
- HBM 8-KV for all pins

3 Pin Definition

3.1 Pin Assignments

Figure 3-1 CS5212 Pin Layout



3.2 Pin Description

Table 3-1 CS5212 Pin Definitions

Pin #	Description	Type	Note
1	AVCC_33	P	Analog power at 3.3V
2	AUX_P	AIO	DP AUX channel positive
3	AUX_N	AIO	DP AUX channel negative
4	NC	--	Reserved
5	LANEO_P	AI	DP Rx lane0 positive
6	LANEO_N	AI	DP Rx lane0 negative
7	LANE1_P	AI	DP Rx lane1 positive
8	LANE1_N	AI	DP Rx lane1 negative
9	POL2	I	Power on latch selection
10	POL1/SPI_CEB	I/O	Power on latch selection or SPI_CEB (flash mode)
11	GPI1/SPI_CLK	I/O	GPI_1 (ROM mode) or SPI_CLK (flash mode)
12	GPI2/SPI_SI	I/O	GPI_2 (ROM mode) or SPI_SI (flash mode)
13	GPI3/SPI_SO	I/O	GPI_3 (ROM mode) or SPI_SO (flash mode)
14	VCC_33	P	Digital power at 3.3V
15	VGA_SCL	O	VGA DDC clock, 5V tolerance (open-drain)
16	VGA_SDA	O	VGA DDC data, 5V tolerance (open-drain)
17	HVSYNC_PWR	P	Power for embedded H/V sync buffer (3.3V or 5V optional)
18	VSYNC	O	VGA vertical sync output (3.3V or 5V output)
19	HSYNC	O	VGA horizontal sync output (3.3V or 5V output)
20	VDD_DAC_33	P	Analog power at 3.3V
21	BLUE_P	AO	VGA blue channel output
22	GREEN_P	AO	VGA green channel output
23	RED_P	AO	VGA red channel output
24	GND	G	Ground
25	VCCK_12	P	1.2V LOD output ping
26	PVCC_33	P	LDO power source at 1.2V
27	GPIO_0	I/O	General IO 0
28	EXT_CLK_IN	I	external reference clock (optional)
29	SMB_SDA	I/O	I2C salve data, 5V tolerance (open-drain)
30	SMB_SCL	I/O	I2C salve clock, 5V tolerance (open-drain)
31	GPIO_4	I/O	General IO 4
32	HPD	O	DP hot plug detection, 5V tolerance

4 Interfaces and Capability

4.1 DisplayPort Input

As a standard DisplayPort receiver, CS5212 consists of two-lane Main Link differential pair, one AUX channel differential pair, and one HPD signal.

- **Main Link**

Two lanes differential pair capable of operating HBR (2.7-Gbps) and RBR (1.62-Gbps) data rates for high definition uncompressed video transmission. The main link is fully compliant with the DisplayPort v1.1 specification.

- **AUX Channel**

A differential half-duplex bi-directional channel used for side-band communication between the DisplayPort source and sink devices. The bandwidth of this link is up to 1-Mbps.

- **Hot Plug Detect (HPD)**

The HPD signal is fully compliant with the DisplayPort v1.1. This includes all input voltage requirements and generation of hot plug and IRQ_HPDP events.

4.2 Analog VGA output

CS5212 integrates triple 8bit-210MHz-DAC (Digital-to-Analog Converters), with each DAC assigned for each color, R (red), G (green), and B (blue). The Analog VGA interface of CS5212 is compliant with the VESA VSIS v1r2. Real-time Hot plug detection mechanism is also integrated into CS5212.

The most popular video formats supported by CS5212 are shown in the following Table 2. However, the formats supported by CS5212 are not limited to this table. Those formats with (a) the data transmission bandwidth lower than the maximal bandwidth of 2-lane DisplayPort HBR main-link and (b) the pixel frequency slower than the maximal DAC speed 210-MHz can also be supported by CS5212.

Table 4-1 Supported Popular Timing/ Resolution

Resolution	Refresh Rate (Hz)	Horizontal Freq. (kHz)	Pixel Freq. (MHz)	Standard Type	Ori. Document	Date
640 x 350	85	37.9	31.500	VESA Standard	VDMTPROP	3/1/96
640 x 400	85	37.9	31.500	VESA Standard	VDMTPROP	3/1/96
720 x 400	85	37.9	31.500	VESA Standard	VDMTPROP	3/1/96
640 x 480	60	31.5	25.175	Industry Standard		
	72	37.9	31.500	VESA Standard	VS901101	12/2/92
	75	37.5	31.500	VESA Standard	VDMT75HZ	10/4/93
	85	43.3	36.000	VESA Standard	VDMTPROP	3/1/96
800 x 600	60	37.9	40.000	VESA Guidelines	VG900602	8/6/90
	72	48.1	50.000	VESA Standard	VS900603A	8/6/90
	75	46.9	49.500	VESA Standard	VDMT75HZ	10/4/93
	85	53.7	56.250	VESA Standard	VDMTPROP	3/1/96
848 x 480	60	31.0	33.750	VESA Standard	AddDMT	3/4/03
1024 x 768	43 (Int.)	35.5	44.900	Industry Standard		
	60	48.4	65.000	VESA Guidelines	VG901101A	9/10/91
	70	56.5	75.000	VESA Standard	VS910801-2	8/9/91
	75	60.0	78.750	VESA Standard	VDMT75HZ	10/4/93
	85	68.7	94.500	VESA Standard	VDMTPROP	3/1/96
1152 x 864	75	67.5	108.000	VESA Standard	VDMTPROP	3/1/96
1280 x 720	60	45.0	74.250	CEA Standard	CEA -861	
1280 x 768	60 (RB)	47.4	68.250	CVT Red. Blanking	AddDMT	3/4/03
	60	47.8	79.500	CVT	AddDMT	3/4/03
	75	60.3	102.250	CVT	AddDMT	3/4/03
	85	68.6	117.500	CVT	AddDMT	3/4/03
	60 (RB)	49.3	71.000	CVT Red. Blanking	CVT1.0 2MA-R	5/1/07
1280 x 800	60	49.7	83.500	CVT	CVT 1.02MA	5/1/07
	75	62.8	106.500	CVT	CVT 1.02MA	5/1/07
	85	71.6	122.500	CVT	CVT 1.02MA	5/1/07
	60	60.0	108.000	VESA Standard	VDMTPROP	3/1/96
1280 x 960	85	85.9	148.500	VESA Standard	VDMTPROP	3/1/96
	60	64.0	108.000	VESA Standard	VDMTREV	12/18/96
1280 x 1024	75	80.0	135.000	VESA Standard	VDMT75HZ	10/4/93
	85	91.1	157.500	VESA Standard	VDMTPROP	3/1/96
	60 (RB)	48.0	72.000	VESA Standard	DMT Update	11/30/07
1360x768	60	47.7	85.500	VESA Standard	AddDMT	3/4/03
	60	47.7	85.500	VESA Standard	DMT Update	11/30/07
	60 (RB)	64.7	101.000	CVT Red. Blanking	AddDMT	5/13/03
1400 x 1050	60	65.3	121.750	CVT	AddDMT	3/4/03
	75	82.3	156.000	CVT	AddDMT	3/4/03
	85	93.9	179.500	CVT	AddDMT	3/4/03
	60 (RB)	55.5	88.750	CVT Red. Blanking	CVT1.30MA-R	7/14/04
1440 x 900	60	55.9	106.500	CVT	CVT1.30MA-R	7/14/04
	75	70.6	136.750	CVT	CVT1.30MA-R	7/14/04
	85	80.4	157.000	CVT	CVT1.30MA-R	7/14/04
	60 (RB)	60.0	108.000	VESA Standard	VDMTREV	11/17/08
1600 x 900	60	75.0	162.000	VESA Standard	VDMTREV	12/18/96
	65	81.3	175.500	VESA Standard	VDMTREV	12/18/96
	70	87.5	189.000	VESA Standard	VDMTREV	12/18/96
	75	93.75	202.5	VESA Standard	VDMTREV	12/18/96
	60 (RB)	64.7	119.000	CVT Red. Blanking	CVT1.76MA-R	7/14/04
1680 x 1050	60	65.3	146.250	CVT	CVT1.76MA-R	7/14/04
	75	82.3	187.000	CVT	CVT1.76MA-R	7/14/04
	60	67.5	148.500	CEA Standard	CEA -861	-
1920 x 1080	60 (RB)	74.0	154.000	CVT Red. Blanking	AddDMT	3/4/03
1920 x 1200	60	74.6	193.250	CVT	AddDMT	3/4/03
	60 (RB)	88.822	184.750	CVT Red. Blanking	CVT2.76M3-R	-
2048 x 1152	60 (RB)	70.992	156.750	CVT Red. Blanking	VDMT REV	11/17/08
2048 x 1536	60 (RB)	94.769	209.250	CVT Red. Blanking	CVT3.15M3-R	-
2560 x 1080	60 (RB)	66.636	181.250	Cinema 21:9 Aspect Ratio	N/A	N/A

5 Electrical Specifications

5.1 Absolute Maximum Conditions

Permanent damage may occur if absolute maximum conditions are violated. Refer to Section 5.2 for functional operating limits.

Table 5-1 Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Unit
DVCC33	Digital I/O supply voltage	-0.3	—	3.96	V
AVCC33	Analog I/O supply voltage	-0.3	—	3.96	V
VDD_DAC_33	DAC supply voltage	-0.3	—	3.96	V
HVSYNC_PWR	H/V sync buffer voltage (3.3V output)	-0.3	—	3.96	V
	H/V sync buffer voltage (5V output)	-0.3	—	6	V
T _J	Junction temperature	-40	—	125	°C
T _{STG}	Storage temperature ¹	-65	—	150	°C
ESD _{HBM}	ESD protection (Human body model)	—	—	±8	KV
ESD _{CDM}	ESD protection (Charge Device model)	—	—	700	V

1. Max 260°C can be guaranteed with max 8 sec soldering time.

5.2 Operating Conditions

Table 5-2 Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
DVCC33	Digital I/O supply voltage	3.0	3.3	3.6	V
AVCC33	Analog I/O supply voltage	3.0	3.3	3.6	V
VDD_DAC_33	DAC supply voltage	3.0	3.3	3.6	V
HVSYNC_PWR	H/V sync buffer voltage (3.3V output)	3.0	3.3	3.6	V
	H/V sync buffer voltage (5V output)	4.75	5	5.25	V
T _A	Ambient temperature	-10	—	70	°C
Q _{JA}	Package thermal resistance, no air flow	—	39.3	—	°C/W

5.3 Electrical Specification

Table 5-3 DC Electrical Specification

Symbol	Parameter	For 3.3V I/O		
		Min	Typ	Max
V _{il} (V)	Input low voltage	—	—	0.8

Symbol	Parameter	For 3.3V I/O		
		Min	Typ	Max
V _{ih} (V)	Input high Voltage	2.0	—	—
V _{ol} (V)	Output low voltage	0	—	0.4
V _{oh} (V)	Output high voltage ¹	2.4	—	—
I _{in} (uA)	Input leakage current	-10	—	+10
I _{hiz} (uA)	Output tri-state leakage current	-10	—	+10

Table 5-4 AC Electrical Specification

Symbol	Description	Min	Typ	Max	Unit
UI _{High_Rate}	Unit Interval for High Bit Rate (2.7Gbps/lane)		370		ps
UI _{High_Rate}	Unit Interval for High Bit Rate (1.62Gbps/lane)		617		ps
t _{RX-EYE_CONN}	Minimum Receiver Minimum Eye Width at Rx-side connect pins	0.51			UI
t _{RX-EYE_CONN}	Minimum Receiver Minimum Eye Width at Rx package pins	0.47			UI
T _{RX-EYE-MEDIAN-to-MAX- JITTER_CHIP}	Maximum time between the jitter median and maximum deviation from the median at Rx package pins			0.265	UI
L _{RX-SKEWINTER_PAIR}	Lane-to-Lane Skew at RX package pins			5200	ps
L _{RX-SKEWINTRA_PAIR High-Bit-Rate}	Lane Intra-pair Skew at RX package pins			100	ps
L _{RX-SKEWINTRA_PAIR Reduced-Bit-Rate}	Lane Intra-pair Skew at RX package pins			300	ps
F _{RX-TRACKINGBW}	Jitter Tracking Bandwidth	20			MHz
UI	AUX Unit Interval	0.4	0.5	0.6	us
T _{AUX-BUS-Pre-charge}	Number of pre-charge pulse	10		16	

5.4 CS5212 Power Consumption

Different applications would result in different power consumptions of CS5212. For example, whether to adopt the embedded oscillator, and how fast of the video clock frequency are all definitely the key factors of the power consumption of CS5212. The following tables show the reference power consumption of CS5212 in several different application conditions

Table 5-5 CS5212 Typical Power Consumption

Active Resolution / Standby	DP Config.	Min	Typ	Max	Unit
800x600x60 (74.25-MHz)	1-Lane1.62g	-	323.4	-	mW
1024x768x60 (103-MHz)	1-Lane/2.7g	-	376	-	mW
1920x1080x60 (148-MHz)	2-Lane/2.7g	-	442	-	mW
Stand-by mode	-	-	-	100	uW

Note: In practice, the measured power consumption might be slightly different from the tables above due to the different video content and the different measurement equipment

6 Package Specification

Figure 6-1 CS5212 Package Outline (QFN32 Leads 4x4mm²)

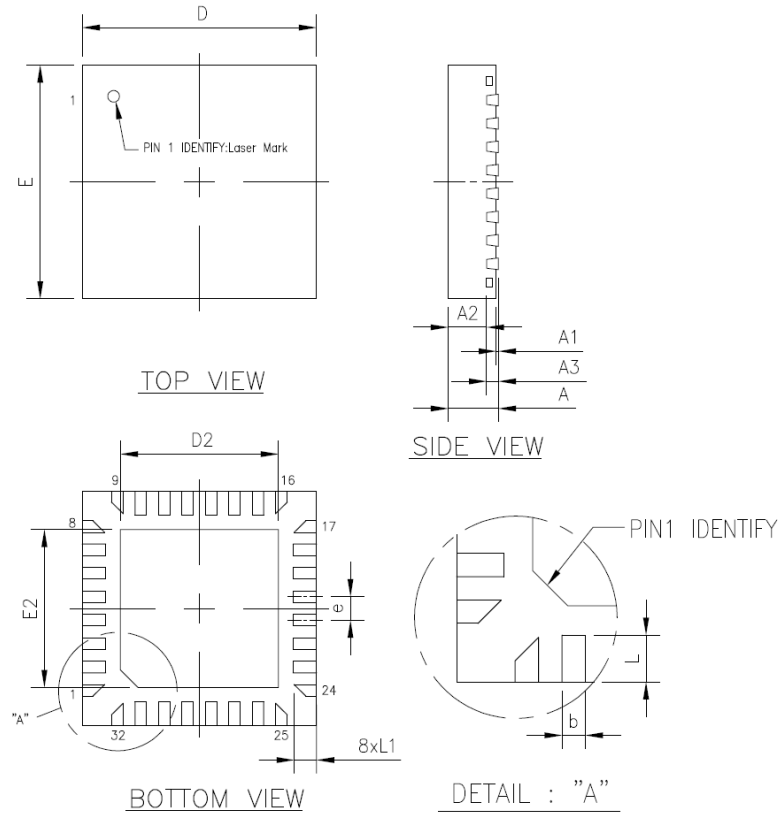


Table 6-1 Package Dimension

Symbol	Dimension in mm			Dimension in inch		
	Min	Normal	Max	Min	Normal	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	—	0.65	0.70	—	0.026	0.028
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.080	0.010
D/E		4.00 BSC			0.157 BSC	
D2/E2	2.55	2.70	2.85	0.096	0.106	0.116
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
L1	0.282	0.382	0.482	0.011	0.015	0.019

7 Ordering Information

The CS5212 can be ordered using the part numbers in Table 7-1. Please consult sales for further details.

Table 7-1 CS5212 Ordering Information

Part No.	Description	Status
CS5212	32 Pin (QFN) package	Sample

8 Revision History

Table 8-1 Document Revision History

Revision	Date	Changes
Release 1	Mar 2020	Initial version
Release 2	May 2020	Update